

- 1.0 IDENTIFICATION
- 1.1 Maindec 702 Revised
- 1.2 PDP-7 Extended Checkerboard
- 1.3 May 16, 1966

2. ABSTRACT

The PDP-7 Extended Checkerboard verifies the performance of from 4096 to 32,768 words of core memory and its associated logic. Memory is exercised in 4096 word increments with four test patterns and their complement patterns. The program resides in the lower addresses of the first 4K of memory and relocates to enable exercising of that region of memory.

3. REQUIREMENTS

3.1 Storage

The program, when initially loaded, occupies locations 0020 to 0474.

3.2 Subprograms (None)

3.3 Equipment

Standard PDP-7 with 4096 to 32,768 words of memory.

3.4 Miscellaneous (Not Applicable)

4. USAGE

4.1 Loading

The binary tape is punched in HRI mode.

AC sw Set the AC switches to 000000₈.

ADDRESS sw Set the Address switches to 00020₈.

If extended memory is to be tested set the EXTEND mode switch up; otherwise the switch must be down.

Place the HRI mode binary tape in the reader.

Press READ-IN.

The binary tape is read in HRI mode. At the completion of program load, the test will determine memory size and initiate memory (see section 4.4 for Start-Up and/or Entry).

NOTE: With the EXTEND mode switch down, the PDP-7 Extended Checkerboard may be loaded into any of the extended 8K areas and only that area will be tested. At the time of load, with the EXTEND mode switch down, the ADDRESS switches may be set to any of the following octal settings.

HRI LOAD ADDRESS

00020	TEST	00000 to 17777
20020	TEST	20000 to 37777
40020	TEST	40000 to 57777
60020	TEST	60000 to 77777

With the EXTEND mode switch up, the only address the program may be loaded at is 00020.

4.2 Calling Sequence (Not Applicable)

4.3 Switch Settings

4.3.1 ADDRESS SWITCHES

Loading Address 00020 (or see section 4.1 for loading into extended memory and not in EXTEND mode).

4.3.2 EXTEND Switch

Up - to test extended memory with Checkerboard in the first 4K.

Down - for all other cases.

4.3.3 AC Switches

Up - Suppress writing the corresponding bit as a 1 in memory and do not test that bit for failure.

Down - Include the corresponding bit in generating patterns and test it for failure.

4.4 Start-Up and/or Entry

When the Checkerboard program is read in, it is automatically started at address 0020 by the memory sizing routine. The first 4K of memory tested is addresses 10000 to 17777 (or 0400 to 7777 if only a 4K machine). The program then relocates to starting address 10020 (or 7420 if only a 4K machine) and tests the lowest 4K of memory, addressing 00000 to 07777 (or 0000 to 7377 if only a 4K machine). The Checkerboard will have one of three addresses for restart, depending on machine size and where the program was located at the time it was halted.

Set ADDRESS switches to 00020
7420
or 10020

AC switches - down - to test all bits
- up - to suppress testing

Press START

NOTE: The above addresses are also relative to the 8K of extended memory into which the program is loaded.

4.5 Errors in Usage

The following halts occur in succession for each error:

HALT 1

C(MA) = 00225, 07625 or 10225

C(AC) = contents of failed register

At least one bit in the memory cell just examined was not in its proper state. Each such bit in error appears as the complement of the majority of bits. Suppressed bits appear as 0s even though they might be 1s in the memory location.

For example, if the contents of the AC = 777767, one of two conclusions may be drawn:

Bit 14 was dropped on the first read/complement.

Bit 14 was picked up on the second read/complement.

Or, the contents of the AC = 000010 bit 14 could have been picked up on the first read/complement or dropped on the second.

Press CONTINUE:

HALT 2

C(MA) = 00227, 07627, or 10227

C(AC) = address of the register causing the previous HALT.

Press CONTINUE:

HALT 3

C(MA) = 00231, 07631, or 10231

C(AC) = control word used to generate the current memory pattern.

4.6 Recovery from Such Errors

HALT 1: Press CONTINUE for next HALT

HALT 2: Press CONTINUE for next HALT

HALT 3: Press CONTINUE to resume testing

5. RESTRICTIONS

The EXTEND mode switch must be down if the Checkerboard is to be loaded and run outside the first 8K of memory.

Maindec 703 Memory Address Test should run successfully before this test is attempted on an unknown machine.

6. DESCRIPTION

6.1 General

The PDP-7 Extended Checkerboard is designed to worst-case test core memory in 4K increments with the minimum possibility that the test itself be destroyed by a memory malfunction, and to test memory from minimum to maximum configuration. HRI binary is supplied as an aid to loading the program with a minimum functioning hardware requirement.

At the completion of program load, the memory sizing routine determines if the area the program has been loaded into is 4K or 8K, and adjusts addressing constants if only 4K and Checkerboard is started. If 8K, EXTEND mode is tested and if a 0, the Checkerboard is started. If EXTEND mode is on, the program determines extended memory size and makes two JMP modifications to the basic Checkerboard so that the extended memory test will be moved out of the way and back again while the first 4K of memory is being tested.

Memory is exercised in 4096 word increments. Each 4K of memory is fully tested before the test proceeds to the next 4K. A total of four patterns and their complement patterns are generated, exercised, and tested in each 4K before proceeding to the next 4K.

6.1.1 Pattern Description

The Extended Checkerboard generates and exercises four basic patterns and their complement patterns. These patterns would appear in a bit plane as follows:

Pattern 1:

		X						X			
		0 1 2 3						0 1 2 3			
Y	0	1	0	0	1	Y	0	1	1	0	
	1	0	1	1	0		1	0	0	1	
	2	0	1	1	0		1	0	0	1	
	3	1	0	0	1		0	1	1	0	

Pattern 2:

		X						X			
		0 1 2 3						0 1 2 3			
Y	0	1	0	0	1	Y	0	1	1	0	
	1	1	0	0	1		0	1	1	0	
	2	0	1	1	0		1	0	0	1	
	3	0	1	1	0		1	0	0	1	

Pattern 3:

		X						X			
		0 1 2 3						0 1 2 3			
Y	0	1	1	0	0	Y	0	0	1	1	
	1	1	1	0	0		0	0	1	1	
	2	0	0	1	1		1	1	1	0	0
	3	0	0	1	1		1	1	1	0	0

Pattern 4:

		X						X			
		0 1 2 3						0 1 2 3			
Y	0	1	1	0	0	Y	0	0	1	1	
	1	0	0	1	1		1	1	1	0	0
	2	0	0	1	1		1	1	1	0	0
	3	1	1	0	0		0	0	1	1	

These patterns are generated by a common routine that produces them by using a different 18-bit control word for each pattern. Bit 0 to bit 15 of the control word generate 16 consecutive pattern words. If a bit is a 0, a word of all 0s is written into the corresponding memory location; if a 1, a word of all 1s is written. In bit 17 of the control word, a 1 indicates that the pattern complements on X addresses 100, 300, 500, and 700 (see patterns 1 and 2). In bit 17 of the control word, a 0 indicates that the pattern complements on X addresses 000, 200, 400, and 600 (see patterns 3 and 4).

The control words used to generate the patterns are as follows:

Pattern 1: 463145

Pattern 2: 631461

Pattern 3: 631460

Pattern 4: 463144

6.1.2 Test Description

Each of the four patterns and its complement pattern is exercised in the same manner. First, the pattern is generated in the memory area being tested. Then, each memory location is individually read, complemented, read, and re-complemented to its original value so that the area being tested still contains the entire pattern. The results of the second read are tested for all 1s or all 0s. Then, the pattern is regenerated and each memory register is read; bit 17 is complemented, read, and re-complemented, and the results of the second read are tested for all 0s or all 1s. The pattern is regenerated and bit 16 is tested, then bit 15, and the process is repeated until bit 0 has been tested.

6.2 Applications

The Extended Checkerboard is designed for a minimum of manual intervention in completely exercising all available memory. Most other applications require manual intervention and the changing of the contents of specific memory locations.

Some of these applications can be accomplished as follows:

To Select a Single Pattern:

To exercise memory with only one of the four patterns it is necessary to change four memory locations so that they contain the same control word, i.e., all four memory locations should equal 463145 to exercise pattern 1 only.

<u>Addresses</u>	<u>Current Contents</u>	<u>Pattern</u>
0271	463145	One
0272	631461	Two
0273	631460	Three
0274	463144	Four

To Prevent Program from Relocating:

At times it may be desirable to exercise a single 4K memory module. In the case of a PDP-7 with only 4K of memory, one may want to only exercise addresses 0400 to 7777 or only addresses 0000 to 7377. This may be accomplished by using one of the following two procedures.

NOTE: The first 4K of memory tested after program load is addresses 10000 to 17777, (or address 0400 to 7777 if only a 4K machine).

To lock the program into exercising only upper addresses:

Press STOP (immediately after loading).

Set ADDRESS switches to 0046, 20046, 40046, or 60046.

Set AC switches to 600020.

Press DEPOSIT (up).

Set AC switches to 000000.

Press START.

After testing the first area, the program relocates itself to starting address 10020 (or 7420 if only 4K). This move can be detected by watching the PROGRAM COUNTER indicators. Bit 2 of the PROGRAM COUNTER will light after the program has been relocated (or bits 3, 4, and 5 if only a 4K machine).

To lock the program into exercising address 00000 to 07777 (or to 7377 if the machine has only 4K)

Load the Extended Checkerboard with all AC switches up.

Watch the PROGRAM COUNTER until the test has relocated itself.

Press STOP.

Set the ADDRESS switches to 10046, 30046, 50046, or 70046 (or if only a 4K machine to 07446).

Set the AC switches to 610020 (or if only a 4K machine to 607420).

Press DEPOSIT (up).

Set AC switches to 000000.

Press START.

Since the Extended Checkerboard can be loaded into and run from extended memory by loading with the EXTEND switch down, these procedures may be used to test any 4K of extended memory.

7. METHODS (Not Applicable)

8. FORMAT (Not Applicable)

9. EXECUTION TIME

Approximately 53 seconds for each 4096 words of memory.

10.	PROGRAM
10.1	Core Map (None)
10.2	Dimension List (None)
10.3	Macro, Parameter, and Variable Lists (None)
10.4	Program Listing

/PDP-7 MEMORY CHECKERBOARD 4K OR 8K AND EXTENDED MEMORY

BITCON	266	NDLOOP	65	PASSK	244
CHKRRD	20	NOXTND	375	MSKOUT	245
CHKRLD	32	ONE	265	TESTWR	246
CNTROL	247	OPRCON	270	CNTROL	247
COFINI	232	PASSK	244	OPRPRD	250
COLOOP	207	PATGEN	261	K16	251
COMEMO	202	PATLOC	236	K200	252
DMPEND	474	SETUP	277	K377	253
EGHTKX	460	STRTAD	276	INDEX	254
FNDLTH	364	SVADRS	255	SVADRS	255
FOURKX	457	SVLGTH	256	SVLGTH	256
GENPAT	130	SVMSTR	240	TESTWR	257
GETPAT	260	SXTNKX	462	GETPAT	260
GNILOP	152	TEST	104	PATGEN	261
KCNTR	466	TESTND	60	K100	262
KCOUNT	465	TESTWR	246	LWR	263
KLENTH	323	TESTWR	257	OPR	264
K100	262	TSXTND	325	ONE	265
K10000	467	TWLVKX	461	BITCON	266
K16	251	TWTKX	463	MLENTH	267
K200	252	OPR	264	OPRCON	270
K377	253	OPRPRD	250	MSTRPT	271
K400	322	OPRSTR	241	STRTAD	276
K7400	324	XIDTST	377	SETUP	277
K7777	470	XINDLP	416	K400	322
LASTKX	464	CHKRRD	20	KLENTH	323
LWR	263	CHKRLD	32	K7400	324
MADDRS	242	MVLOOP	46	TSXTND	325
MIN4	243	TESTND	60	FNDLTH	364
MLENTH	267	NDLOOP	65	NOXTND	375
MOVBAK	442	MVJMP1	100	XIDTST	377
MOVEK1	471	MVJMP2	103	XINDLP	416
MOVEK2	472	TEST	104	MOVEUP	427
MOVEK3	473	GENPAT	130	MOVBAK	442
MOVEUP	427	GNILOP	152	MVJMPS	455
MSKOUT	245	COMEMO	202	FOURKX	457
MSTRPT	271	COLOOP	207	EGHTKX	460
MVJMPS	455	COFINI	232	TWLVKX	461
MVJMP1	100	PATLOC	236	SXTNKX	462
MVJMP2	103	SVMSTR	240	TWTKX	463
MVLOOP	46	OPRSTR	241	LASTKX	464
NDEX	254	MADDRS	242	KCOUNT	465
		MIN4	243		

KCNTR 466
 K10000 467
 K7777 470
 MOVEK1 471
 MOVEK2 472
 MOVEK3 473
 DMPEND 474

/PDP-7 MEMORY CHECKERBOARD 4K OR 8K AND EXTENDED MEMORY

20/

```

CHKRBD,      LAC .
              DAC STRTAD      /GET REGION S.A.
              DAC MADDRS     /TO START TESTING
              LAS
              CMA
              DAC MSKOUT
              LAC MIN4        /-4
              DAC PASSK      /TO COUNT PATTERNS
              LAC PATLOC
              DAC GETPAT      /TO GET PATTERNS

CHKRLP,      LAC I GETPAT     /GET NEXT CHECKERBOARD
              DAC CNTR0L     /FOR GENERATING
              JMS TEST        /TEST CURRENT REGION
              ISZ GETPAT
              ISZ PASSK      /DONE ALL 4 CHECKERBOARDS
              JMP CHKRLP     /NO, DO NEXT
              DZM MSKOUT
              DZM NDEX
              LAC CHKRBD     /GET SA OF THIS PROGRAM
              DAC GETPAT     /FOR INDIRECTS

/MOVE THE PROGRAM TO TEST MEMORY NOT TESTED ON THE LAST PASS
              XOR UPRPRO     /CHANGE S.A. TO NEXT TEST
              DAC SVADRS     /FOR INDIRECTS
MVLOOP,      LAC I GETPAT     /GET NEXT INSTR
              AND OPRCON     /740000
              SAD OPRCON     /IS IT AN OPERATIVE INSTR
              JMP TSTEND     /MAYBE
              LAC I GETPAT
              XOR UPRPRO     /CHANGE ADDRESS OF REF.

              DAC I SVADRS
              ISZ SVADRS     /ADVANCE
              ISZ GETPAT     /ADDRESSES
              JMP MVLOOP

TSTEND,      LAC I GETPAT
              DAC I SVADRS   /STORE OPERATIVE GROUP
              CMA
              SZA
              JMP TSTEND-3   /DELIMITER
              /NO
  
```

```

NDLOOP,      ISZ GETPAT
              ISZ SVADRS
              LAC I GETPAT      /GET NEXT CONSTANT
              DAC I SVADRS
              CMA
              SZA CLA-OPR      /2ND DELIMITER
              JMP NDLOOP       /NO

              ISZ SVADRS      /ADVANCE FOR STORE S.A.
              DAC I SVADRS    /MAKE SA=LWR START
              SAD MADDRS     /THIS TEST TESTING LWR
              SKP            /YES, NEXT PASS TEST UPR
              /HAVE EXTENDED MEMORY
MVJMP1,      JMP I TSTLWR     /GO TEST LWR MEMORY OR JMP MOVEUP
              LAC UPRSTR
              DAC I SVADRS    /MAKE S.A. = UPR START

MVJMP2,      JMP I TSTUPR    /GO TEST UPPER MEMORY OR JMP MOVBAK
              /MOVE EXTENDED CHECKERBD BACK

```

/CONNECT SUBROUTINES TO FORM TEST

```

TEST,        JMP .
              JMS GENPAT      /GENERATE PATTERN
              CLA CMA-OPR
              DAC BITCON     /COMPLIMENT WHOLE WORDS
              JMS COMEMO     /COMPLIMENT AND COMPARE
              LAC ONE
              DAC BITCON     /COMPLIMENT SINGLE BITS
              JMS GENPAT     /GENERATE
              JMS COMEMO     /COMPLIMENT AND COMPARE
              LAC BITCON
              CLL RAL-OPR    /NEXT BIT
              DAC BITCON
              SZA            /DONE ALL
              JMP .-6       /TEST NEXT BIT
              LAC MIN4
              XOR I GETPAT
              SAD CNTROL     /DONE COMPLIMENT PATTERN
              JMP I TEST     /YES
              DAC CNTROL
              JMP TEST+1

```

/PATTERN GENERATION VARIABLE LENGTH
/AND PATTERN CONTROLLED BY INITIAL
/CONTENTS OF CONTROL

```

GENPAT,      JMP .
              LAC CNTROL     /GET MASTER PATTERN WORD
              DAC SVMSTR
              RAR
              LAC K100
              SNL
              CLA
              DAC LWR
              TAD K200
              DAC UPR

```

```

LAC MADDRS
DAC SVADRS           /SAVE STARTING ADDRESS
LAC MLENTH
DAC SVLGTH           /NUMBER OF WORDS

LAC K16              /-16 DECIMAL
DAC NDEX
LAC SVMSTR
DAC PATGEN           /RESET FOR PATTERN
GNLOOP, LAC PATGEN
CLL RAL-OPR         /NEXT BIT TO LINK
DAC PATGEN           /SAVE REST
SZL CLA-OPR         /SHOULD NEXT WORD = 0

CMA                  /NO
AND MSKOUT          /CLR NOT SELECT
DAC I SVADRS
ISZ SVADRS          /GENERATE NEXT ADDRESS
ISZ SVLGTH          /DONE WHOLE PATTERN
SKP
JMP I GENPAT        /EXIT
ISZ NDEX            /DONE 16 WORDS
JMP GNLOOP         /NO

LAC SVADRS
AND K377            /CLR NEXT ADDRS TO LWR 8
SAD LWR
JMP .+4             /IF = 0
SAD UPR             /OR = 200
SKP                 /COMPLIMENT MASTER PAT
JMP GNLOOP-4
LAC SVMSTR
CMA
DAC SVMSTR
JMP GNLOOP-4       /DO NEXT 200

/COMPARE MEMORY FOR FAILURE
COMEMO, JMP .
LAC MADDRS
DAC SVADRS           /SAVE STARTING ADDRESS
LAC MLENTH
DAC SVLGTH           /SAVE LENGTH
COLOOP, LAC BITCON
XOR I SVADRS
DAC I SVADRS
LAC BITCON
XOR I SVADRS
DAC I SVADRS

AND MSKOUT          /CLR NOT SELECTED BITS
SZA                 /IF -

CMA                 /MAKE +
AND MSKOUT          /CLR AGAIN
SNA                 /RESULT SHOULD BE 0
JMP COFINI

```

```

CMA
AND MSKOUT
HLT
LAC SVADRS           /DISPLAY FAILED BIT 8S9
HLT
LAC CNTRL
HLT                 /DISPLAY PATTERN CON.WORD
COFINI,             ISZ SVADRS
                   ISZ SVLGTH           /DO ALL
                   JMP COLOOP          /NO
                   JMP I COMEMO

```

PATLOC, MSTRPI

/CONSTANTS NOT CHANGED BY MOVING THE PROGRAM
/AND TEMP STORE REGISTERS

	I AM	/DELIMITER
SVMSTR,	Ø	/TO GENERATE PATTERNS
UPRSTR,	10000	/S.A. TO TEST UPR MEM
NADRS,	Ø	/TEMP STOR CURRENT REGION
MIN4,	777774	/-4
PASSK,	Ø	/TO COUNT PATTERNS
MSKOUT,	Ø	/TO NOT COMPARE BITS
TESTLWR,	10000+CHKRBD	/TO START TEST ON LOWER
CNTRL,	Ø	/TO STORE CURRENT PATTERN
UPRPRD,	10000	/MASK TO MOVE PROGRAM
K16,	777760	/TO COUNT WORDS IN GENPAT
K200,	200	/TO FORM 200 OR 300
K377,	377	/TO MASK ADDRESSES
INDEX,	Ø	/FOR COUNTING
SVADRS,	Ø	/FOR INDIRECTS
SVLGTH,	Ø	/TO COUNT MEM LENGTH
TESTUPR,	CHKRBD	/TO START TEST ON UPR
GETPAT,	Ø	/FOR INDIRECTS
PATGEN,	Ø	/USED IN GENERATING
K100,	100	/TO FORM 100 AND 300
LWR,	Ø	/= 0 OR 100
UPR,	Ø	/= 200 OR 300
ONE,	1	
BLTCON,	Ø	
MLENTH,	770000	/LENGTH OF MEM TO TEST
UPRCON,	740000	
MSTRPI,	463145	/GENERATE PATTERN 1
	631461	/GENERATE PATTERN 2
	631460	/GENERATE PATTERN 3
	463144	/GENERATE PATTERN 4

	L AM	/DELIMITER
STRTAD,	10000	

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/TEST MEMORY LENGTH AND ADJUST
/TEST CONSTANTS IF ONLY 4K

```
SETUP,      CAF
            DZM 7777
            CLA CMA-OPR
            DAC 17777
            SAD 7777          /IS MEM 4K OR 8K
            JMP .+4          /4K
            SEM
            JMP CHKRBD
            JMP TSXTND
            LAC K400
                                /8K, SEE IF MEMORY IS EXTENDED
                                /CHANGE CONSTANTS

            DAC STRIAD
            DAC UPRSTR
                                /TO TEST 4K MACHINE

            LAC KLENTH
            DAC MLENTH

            LAC K7400
            DAC UPRPRO
            TAD TSTUPR
            DAC TSTLWR

            JMP CHKRBD
            400
            K400,          770400          /4K - 400
            KLENTH,      7400          /MOVE
            K7400,
```

/EXTENDED MEMORY CHECKERBOARD
/DETERMINE MEMORY LENGTH

```
TSXTND,    CLA
            DAC 7777
            DAC 17777
            DAC KCOUNT
            CMA
            EEM
            DAC I FOURKX
            SAD 7777
            JMP NOXTND
            ISZ KCOUNT          /INDICATE EXTENDED 4K
            DAC I EGTKX
            SAD 17777
            JMP FNDLTH          /12K MACHINE (EXTRA 4K)
            ISZ KCOUNT          /INDICATE EXTENDED 8K
            DAC I TWLVKX
            SAD 7777

            JMP FNDLTH          /16K MACHINE (EXTRA 8K)
            ISZ KCOUNT          /INDICATE EXTENDED 12K
            DAC I SIXTKX
            SAD 17777
            JMP FNDLTH          /20K MACHINE (EXTRA 12K)
            CLA
            ISZ KCOUNT          /INDICATE EXTENDED 16K
```

```

DZM I TWYKX
SAD I FOURKX
JMP FNDLTH          /24K MACHINE (EXTRA 16K)
ISZ KCOUNT
DZM I LASIKX
SAD I EGHTKX
JMP FNDLTH          /28K MACHINE (EXTRA 20K)
ISZ KCOUNT          /INDICATE 32K OF CORE

FNDLTH,             CLA CMA-OPR
                   TAD KCOUNT
                   CMA
                   DAC KCOUNT          /MAKE 2'S COMPLIMENT
                   LAC MVJMPS          /OF 4K EXTENDED MODULES
                   DAC MVJMP1
                   LAC MVJMPS+1
                   DAC MVJMP2
                   JMP CHKRBD

NOXTND,            LEM
                   JMP CHKRBD          /CLEAR EXTEND MODE
                                           /NO EXTENDED MEMORY

XTDTST,            LAC KCOUNT
                   DAC KCNTR
                   LAC K10000
                   DAC MADDRS
                   LAC MADDRS
                   TAD K7777
                   DAC MADDRS          /GENERATE S.A. FOR
                   ISZ MADDRS          /NEXT 4K MODULE
                   LAC MIN4           /TO TEST
                   DAC PASSK
                   LAC PATLOC
                   DAC GETPAT
                   LAS
                   CMA
                   DAC MSKOUT
XTNDLP,            LAC I GETPAT
                   DAC CNTR0L
                   JMS TEST
                   ISZ GETPAT
                   ISZ PASSK
                   JMP XTNDLP
                   ISZ KCNTR
                                           /DONE ALL EXTENDED
                   JMP XTDIST+4        /NO, DO NEXT 4K
                   JMP CHKRBD          /YES, TEST 10000 TO 17777
/MOVE THE EXTENDED MEMORY CHECKERBOARD
/OUT OF THE WAY TO TEST BLOCK 0000 TO 7777

MOVEUP,            LAC MOVEK1
                   DAC 10
                   LAC MOVEK2
                   DAC 11
                   LAC MOVEK3
                   DAC SVLGTH
                   LAC I 10
                   DAC I 11
                   ISZ SVLGTH
                   JMP .-3
                   JMP I TSTLWR

```

/MOVE THE EXTENDED MEMORY CHECKERBOARD
/BACK TO FIRST 4K

```

MOVBAK,      LAC MOVEK2+10000    /THIS ROUTINE IS
              DAC 10             /EXECUTED OUT
              LAC MOVEK1+10000   /OF 2ND 4K OF
              DAC 11             /NOT EXTENDED
              LAC MOVEK3+10000   /MEMORY
              DAC SVLGTH+10000
              LAC I 10
              DAC I 11
              ISZ SVLGTH+10000
              JMP .-3+10000
              JMP XTDIST

MVJMPS,      JMP MOVEUP
              JMP MOVBAK

FOURKX,      27777                /TO GET TO FIRST 4K EXTENDED
EGHTKX,      37777                /DITTO  2ND 4K EXTENDED
TWLVKX,      47777                /3RD
SXTNKX,      57777                /4TH
FWTYKX,      67777                /5TH
LASTKX,      77777                /6TH, OR 32K
KCOUNT,     0
KCNTR,       0

K10000,      10000
K7777,       7777
MOVEK1,      XTDIST-1
MOVEK2,      XTDIST+7777
MOVEK3,      -MOVEK3+XTDIST

DMPEND,      JMP SETUP

START

```

10.5 Octal Dump

00000 TO 00006 000000
00007 010153
00010 TO 00017 000000
00020 200020
00021 200276
00022 040242
00023 750004
00024 740001
00025 040245
00026 200243
00027 040244
00030 200236
00031 040260
00032 220260
00033 040247
00034 100104
00035 440260
00036 440244
00037 600032
00040 140245
00041 140254
00042 200020
00043 040260
00044 240250
00045 040255
00046 220260
00047 500270
00050 540270
00051 600060
00052 220260
00053 240250
00054 060255
00055 440255
00056 440260
00057 600046
00060 220260
00061 060255
00062 740001
00063 740200
00064 600055
00065 440260
00066 440255
00067 220260
00070 060255
00071 740001
00072 750200
00073 600065
00074 440255
00075 060255
00076 540242
00077 741000
00100 620246
00101 200241
00102 060255
00103 620257

00104 600104
00105 100130
00106 750001
00107 040266
00110 100202
00111 200265
00112 040266
00113 100130
00114 100202
00115 200266
00116 744010
00117 040266
00120 740200
00121 600113
00122 200243
00123 260260
00124 540247
00125 620104
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020035

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